

Appl. No. 10/710,437

Amdt. dated January 26, 2006

Reply to Office action of November 01, 2005

**AMENDMENTS TO THE CLAIMS**

1. (Currently Amended) A lumped-element diplexer implemented in a multi-layered substrate comprising:

5 a low-pass filter circuit wherein circuit elements are disposed on a first series of layers of the multi-layered substrate and wherein a first end of the low-pass filter circuit is connected to a first port and a second end of the low-pass filter circuit is connected to a second port;

10 a high-pass filter circuit wherein circuit elements are disposed on a second series of layers of the multi-layered substrate and wherein a first end of the high-pass filter circuit is connected to ~~[[a]]~~ the first port and a second end of the high-pass filter circuit is connected to a third port; and

15 a ground plane forming a base of the multi-layered substrate, wherein elements of the filter circuits are orientated horizontally with respect to the ground plane and are arranged in layers aligned substantially vertically, these layers being separated by a dielectric material and inter-layer connections being implemented by at least a via;

20 wherein no layer is between an uppermost layer of the first series of layers of the multi-layered substrate ~~is immediately adjacent to~~ and a lowermost layer of the second series of layers of the multi-layered substrate.

2. (Cancelled)

- 25 3. (Currently Amended) The lumped-element diplexer implemented in a multi-layered substrate of claim 1, wherein:

the low-pass filter circuit comprises:

a first capacitor plate disposed on a first layer of the multi-layered substrate;

a second capacitor plate disposed on a second layer of the multi-layered

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substrate; and

a first inductor plate directly disposed on a third layer of the multi-layered substrate;

wherein the first capacitor plate is connected to the first port, the second capacitor plate is connected to a first end of the first inductor plate and the second port via a third capacitor plate of the high-pass filter circuit, and a second end of the first inductor plate is connected to the first port; and

the high-pass filter circuit comprises:

a third capacitor plate disposed on a ~~forth~~ fourth layer of the multi-layered substrate;

a fourth capacitor plate disposed on a fifth layer of the multi-layered substrate;

a fifth capacitor plate disposed on a sixth layer of the multi-layered substrate; and

a second inductor plate directly disposed on a seventh layer of the multi-layered substrate;

wherein the third capacitor plate is connected to the second port, the

~~forth~~ fourth capacitor plate is connected to a first end of the second

inductor plate, the fifth capacitor plate is connected to the third port and

a second end of the second inductor plate is connected to the ground plane.

4. (Currently Amended) The lumped-element diplexer implemented in a multi-layered substrate of claim 1, wherein ~~inductive~~ the circuit elements of the filter circuits comprise inductive elements that comprise plates formed as spirals.

5. (Currently Amended) The lumped-element diplexer implemented in a multi-layered

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substrate of claim 1, wherein the circuit elements of the filter circuits comprise at least one inductive element ~~of the filter circuits~~ is formed on a plurality of layers of the multi-layered substrate.

- 5     6.     (Currently Amended) The lumped-element diplexer implemented in a multi-layered substrate of claim 1, wherein ~~at least one capacitive element of the circuit elements~~ of the filter circuits comprises comprise at least one capacitive element comprising a plurality of plates formed on a plurality of layers of the multi-layered substrate.
- 10    7.     (Original) The lumped-element diplexer implemented in a multi-layered substrate of claim 1, wherein the high-pass filter circuit further comprises a low frequency notch filter circuit.
- 15    8.     (Currently Amended) The lumped-element diplexer implemented in a multi-layered substrate of claim ~~[[7]]~~ 3, wherein at least the third and fifth capacitor plates are dimensioned to have additional overlapping area in order to realize an additional capacitor equivalence.
- 20    9.     (Currently Amended) The lumped-element diplexer implemented in a multi-layered substrate of claim 1, wherein the ground plane forms a zeroth layer of the lumped-element diplexer.
- 25    10.    (Original) The lumped-element diplexer implemented in a multi-layered substrate of claim 1, wherein the device is realized in a multi-layered, low temperature co-fired ceramic substrate.
11.   (Currently Amended) A lumped-element diplexer implemented in a multi-layered substrate comprising:

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a low-pass filter circuit comprising:

a first capacitor plate disposed on a first layer of a first series of layers of the multi-layered substrate;

5 a second capacitor plate disposed on a second layer of ~~[[a]]~~ the first series of layers of the multi-layered substrate; and

a first inductor plate directly disposed on a third layer of ~~[[a]]~~ the first series of layers of the multi-layered substrate;

wherein the first capacitor plate is connected to a first port, the second

10 capacitor plate is connected to a first end of the first inductor plate and to a second port via a third capacitor plate of a high-pass filter circuit of the lumped-element diplexer, and a second end of the first inductor plate is connected to the first port; and

a high-pass filter circuit comprising:

15 a third capacitor plate disposed on a first layer of a second series of layers of the multi-layered substrate;

a fourth capacitor plate disposed on a second layer of ~~[[a]]~~ the second series of layers of the multi-layered substrate;

a fifth capacitor plate disposed on a third layer of ~~[[a]]~~ the second series of layers of the multi-layered substrate; and

20 a second inductor plate directly disposed on a ~~forth~~ fourth layer of ~~[[a]]~~ the second series of layers of the multi-layered substrate;

wherein the third capacitor plate is connected to the second port, the ~~forth~~

25 fourth capacitor plate is connected to a first end of the second inductor plate, the fifth capacitor plate is connected to a third port and a second end of the second inductor plate is connected to a ground plane of the lumped-element diplexer, and wherein the high-pass filter circuit further comprises a low frequency notch filter circuit realized by additional overlapping area of the third and fifth capacitor plates.

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a ground plane forming a base of the multi-layered substrate, wherein elements of the filter circuits are orientated horizontally with respect to the ground plane and are arranged in layers aligned substantially vertically, these layers being separated by a dielectric material and inter-layer connections being  
5 implemented by at least a via;

wherein no layer is between an uppermost layer of the first series of layers of the multi-layered substrate ~~is immediately adjacent to~~ and a lowermost layer of the second series of layers of the multi-layered substrate.

10 12. (Cancelled)

13. (Currently Amended) The lumped-element diplexer implemented in a multi-layered substrate of claim 11, wherein ~~inductive elements of the filter circuits comprise plates formed as spirals~~ an inductor plate comprises a spiral-shaped metal strip.

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14. (Currently Amended) The lumped-element diplexer implemented in a multi-layered substrate of claim 11, ~~wherein~~ further comprising at least one inductive element ~~of the filter circuits~~ is formed on a plurality of layers of the multi-layered substrate.

20 15. (Currently Amended) The lumped-element diplexer implemented in a multi-layered substrate of claim 11, wherein further comprising at least one capacitive element ~~of the filter circuits comprises a plurality of plates~~ formed on a plurality of layers of the multi-layered substrate.

25 16. (Currently Amended) The lumped-element diplexer implemented in a multi-layered substrate of claim 11, wherein the ground plane forms a zeroth layer of the lumped-element diplexer.